Electronic Version
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Claims

[c1] A method for forming an interconnect structure for a semiconductor device, the method comprising:
defining a via in a passivation layer so as expose a top metal layer in the semiconductor device;
forming a seed layer over said passivation layer, sidewalls of said via, and said top metal layer;
forming a barrier layer over an exposed portion of said seed layer, said exposed portion defined by a first patterned opening of a first diameter; and
forming a solder material over said barrier layer using a second patterned opening of a second diameter;
wherein said second patterned opening is configured such that said second diameter is larger than said first diameter.

[c2] The method of claim 1, further comprising removing exposed portions of said seed layer so as to define a ball limiting metallurgy (BLM), wherein remaining portions of said seed layer do not undercut said barrier layer.

[c3] The method of claim 1, wherein:
said seed layer comprises a titanium-tungsten/chrome-copper/copper (TiW/CrCu/Cu) layer; and

said barrier layer comprises a nickel/copper layer.

[c4] The method of claim 3, wherein copper and chrome copper portions of seed layer are removed by electroetching.

[c5] The method of claim 4, wherein said second diameter exceeds said first diameter by about 20 to about 25 microns.

[c6] A method for forming an interconnect structure for a semiconductor device, the method comprising:
defining a via in a passivation layer so as expose a top metal layer in the semiconductor device;
forming a seed layer over said passivation layer, sidewalls of said via, and said top metal layer;
forming a barrier layer over an exposed portion of said seed layer, said exposed portion defined by a first patterned opening; and
annealing the semiconductor device so as to cause atoms from said barrier layer to diffuse into said seed layer thereunderneath;
wherein said annealing causes diffused regions of said seed layer to have an altered electrical resistivity and electrode potential with respect to undiffused regions of said seed layer.

[c7] The method of claim 6, further comprising etching said

seed layer, following said annealing, so as to define a ball limiting metallurgy (BLM), wherein remaining portions of said seed layer do not undercut said barrier layer.

[c8] The method of claim 6, further comprising:
following said annealing, forming a solder material over said barrier layer using a second patterned opening.

[c9] The method of claim 8, wherein said second patterned opening is configured so as to have a larger diameter than said first patterned opening.

[c10] The method of claim 6, further comprising:
following said annealing, forming a solder material over said barrier layer using said first patterned opening.

[c11] The method of claim 10, wherein said first patterned opening is formed using a photoresist material that is capable of withstanding temperatures generated during said annealing.

[c12] The method of claim 6, wherein said annealing is implemented at a temperature and a duration so as to cause atoms from said barrier layer to diffuse into said seed layer by about one micron in x, y and z-directions.

[c13] The method of claim 12, wherein said annealing results

in an increased electrical resistivity of said diffused regions of said seed layer by about one order of magnitude.

[c14] The method of claim 6, wherein:
said seed layer comprises a titanium-tungsten/chrome-copper/copper (TiW/CrCu/Cu) layer; and
said barrier layer comprises a nickel/copper layer.

[c15] The method of claim 14, wherein copper and chrome copper portions of seed layer are removed by electroetching.

[c16] The method of claim 14, wherein said annealing is implemented at temperature of about 350 to about 380 °C for a duration of about 30 to about 45 minutes.

[c17] A method for introducing a self etch stop mechanism within a metallic thin film, the method comprising:
forming an overlayer upon the thin film;
annealing the thin film so as to cause atoms from said overlayer to diffuse into the thin film thereunderneath;
wherein said annealing causes diffused regions of the thin film to have an altered electrical resistivity and electrode potential with respect to undiffused regions of the thin film.

[c18] The method of claim 17, wherein said annealing is im-

plemented at a temperature and a duration so as to cause atoms from said overlayer to diffuse into the thin film by about one micron in x, y and z-directions.

[c19] The method of claim 18, wherein said annealing results in an altered electrical resistivity and electrode potential of said diffused regions of the thin film by about one order of magnitude.

[c20] The method of claim 17, wherein:
the thin film includes a copper layer; and
said overlayer includes a nickel/copper layer.